REMARKS

Claims 34-38, 45-47 and 53-58 are pending in the present application. Claim 53 has been amended. Claims 54-58 have been presented herewith.

Information Disclosure Statement

The Examiner is respectfully requested to acknowledge receipt of the Information Disclosure Statement filed concurrently herewith, and to confirm that the documents listed therein have been considered and will be cited of record.

Specification

The abstract of the disclosure has been objected to as including reference characters. However, the abstract as amended on pages 9-10 of the Preliminary Amendment filed September 9, 2003, does not include reference numerals. The Examiner is therefore respectfully requested to withdraw the rejection to the abstract for at least these reasons.

Claim Rejections-35 U.S.C. 102

Claims 34-38 and 46 have been rejected under 35 U.S.C. 102(b) as being anticipated by the Lin et al. reference (U.S. Patent No. 5,239,198). This rejection is respectfully traversed for the following reasons.

The semiconductor device of claim 34 includes in combination a BGA (ball grid

array) type semiconductor device; and a CSP (chip size packaged) type semiconductor device "mounted on an area of the backside surface of the base plate of said BGA type semiconductor device which does not have any bumps formed thereon, said CSP type semiconductor device having a semiconductor element which has main and back surfaces, and side surfaces between the main and back surfaces, and a plurality of terminals which are formed on the main surface, wherein the back surface and the entirety of the side surfaces of the semiconductor element are exposed". Applicants respectfully submit that the Lin et al. reference does not disclose these features.

In the Response to Arguments section at the bottom of page 5 of the Final Office Action dated October 28, 2005, the Examiner has asserted that Applicants' previous arguments are not persuasive "because the passive electronic component 50 of the Lin et al. reference is a semiconductor chip comprises a plurality of solder balls 51 (fig. 7, column 6, line 64). Therefore, Lin et al. clearly disclose that the component 50 is a Chip Scale Package (CSP) type".

Applicants respectfully submit that the Examiner has misinterpreted the Lin et al. reference. Particularly, passive electronic component 50 of the Lin et al. reference is not described or even remotely suggested as being "a semiconductor chip", as asserted by the Examiner. As described in column 6, lines 61-66 of the Lin et al. reference "As illustrated in FIG. 6, a passive electronic component 50, such as a resistor, diode, decoupling capacitor, or the like, is electrically coupled to conductive traces 16 by solder joints 51. Electronic component 50 does not need to be overmolded within an

encapsulant".

Accordingly, passive electronic component 50 in Figs. 6 and 7 of the Lin et al. reference is merely a resistor, a diode, a decoupling capacitor, **or the like**. That is, passive electronic component 50 of the Lin et al. reference is a single electronic component, that does not need to be overmolded with encapsulant. There is no description in the Lin et al. reference characterizing passive electronic component 50 as "a semiconductor chip". The Examiner is invited to identify in the Lin et al. reference specific description of passive electronic component 50 as a "semiconductor chip". In this regard, it should be noted that the mere fact that solder balls 51 electrically connect passive electronic component 50 to substrate 12 does not in any way imply that passive electronic component 50 is a semiconductor chip.

It should thus be clear that passive electronic component 50 of the Lin et al. reference is not a CSP type semiconductor device as would be understood by one of ordinary skill. Particularly, CSP type semiconductor devices are understood to be devices that are capable of realizing various sophisticated functions, and are not merely a resistor, a diode, a capacitor, or the like. The Examiner's continued characterization of a passive electronic component such as component 50 of the Lin et al. reference as a CSP semiconductor type device completely disregards and distorts the meaning of a CSP semiconductor type device as would be understood by one of ordinary skill.

Applicants respectfully submit that the Lin et al. reference as relied upon by the Examiner does not disclose a CSP (chip size package) type semiconductor device as

would be necessary to meet the features of claim 34. Applicants therefore respectfully submit that the semiconductor device of claim 34 distinguishes over the Lin et al. reference as relied upon by the Examiner, and that this rejection of claims 34-38 and 46 is improper for at least these reasons.

With further regard to this rejection, the semiconductor device of claim 34 is characterized in that a CSP type semiconductor device is arranged on the rear surface of a base plate of a BGA type semiconductor device. In other words, the space for arranging the semiconductor device can be prevented from being enlarged in view of the high-density packaging by using together different semiconductor device types (BGA and CSP). It is thus possible to provide a high-performance semiconductor device utilizing the functions of these two different semiconductor device types. This prevents size increase, and at the same time enables various sophisticated functions. The Lin et al. reference clearly fails to provide such features, because the Lin et al. reference does not include a CSP type semiconductor device mounted on a BGA type semiconductor device, as would be necessary to meet the features of claim 34.

Claim Rejections-35 U.S.C. 103

Claims 45 and 47 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Lin et al. reference in view of the Schrock reference (U.S. Patent No. 5,861,678). This rejection is respectfully traversed for the following reasons.

The Examiner has acknowledged that the Lin et al. reference fails to disclose a

resin that covers the main surface of the semiconductor element and side surfaces of the terminals, as would be necessary to meet the features of claim 45. The Examiner has relied upon the Schrock reference in an effort to overcome these acknowledged deficiencies.

Applicants respectfully submit that the Schrock reference does not overcome the deficiencies of the Lin et al. reference described above with respect to claim 34. Particularly, the Schrock reference does not disclose a CSP (chip size packaged) type semiconductor device mounted on a backside surface of a base plate of a BGA (ball grid array) type semiconductor device. The Schrock reference does not teach a semiconductor device that achieves high density packaging by using together different semiconductor device types including BGA and CSP type semiconductor devices.

With further regard to this rejection, the Schrock reference simply discloses a technology to be adopted when mounting a die 10 at a substrate 30 as illustrated in Figs. 3 and 4. The Schrock reference does not disclose a BGA type semiconductor device. This is significant because while it may appear that die 10 is merely mounted on the rear surface of substrate 30 of the Schrock reference, die 10 actually needs to be heated via a heater disposed inside the die support frame, whereby a structure such as shown in Fig. 1C of the Schrock reference needs to be achieved. It is not clear how the teachings of the Lin et al. reference as set forth with respect to Figs. 6 and 7 could be modified in view of the above noted teachings of the Schrock reference, which require heating of a die disposed inside a die support frame. Accordingly, Applicant

respectfully submits that claims 45 and 47 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection of claims 45 and 47 is improper for at least these reasons.

Response to Arguments Section

On page 5 of the Final Office Action dated October 28, 2005, the Examiner has cited the Nishi et al. reference (U.S. Patent No. 5,949,140) and the Lee et al. reference (U.S. Patent No. 6,081,037) in an effort to support characterization of passive electronic component 50 of the Lin et al. reference as a semiconductor device. Applicants however emphasize that the semiconductor device according to claim 34 includes two different types of semiconductor devices including a BGA type semiconductor device and a CSP type semiconductor device. The Nishi et al. and the Lee et al. references as relied upon by the Examiner do not establish or even remotely suggest that passive electronic component 50 of the Lin et al. reference may be characterized as a CSP type semiconductor device.

Allowable Subject Matter

Applicants note the Examiner's acknowledgment that claim 53 has been objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form. Claim 53 has been amended to be in independent form responsive to the acknowledgment of allowable subject matter. The Examiner is

respectfully requested to acknowledge that claim 53 is thus allowed.

Claims 54-58

Applicants respectfully submit that claims 54-56 should also be allowable at least by virtue of dependency upon claim 53. Moreover, claims 57 and 58 should define over the relied upon prior art at least by virtue of dependency upon claim 34 for the reasons as set forth above, and by further reasons of the features therein.

Conclusion

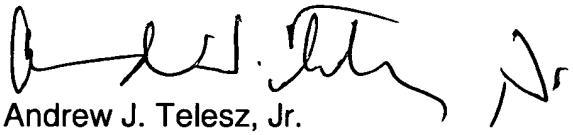
The Examiner is respectfully requested to reconsider and withdraw the corresponding rejections, and to pass the claims of the present application to issue, for at least the above reasons.

In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (571) 283-0720 in the Washington, D.C. area, to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

VOLENTINE FRANCOS & WHITT, P.L.L.C.



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